(Declared u/s 3 of UGC Act, 1956)

Department of Electronics and Communication Engineering

Sub Code/Name: **BEC4L2- LINEAR INTEGRATED CIRCUITS LAB (R)**

Name : ……

Reg No : ……

Branch : ……

Year & Semester : ……

LIST OF EXPERIMENTS

INDEX

Expt.	Date	Name of the Experiment	Marks	Staff SIGN

EX.No:1

Date:

DESIGN AND TESTING OF INVERTING, NON-INVERTING AMPLIFIERS

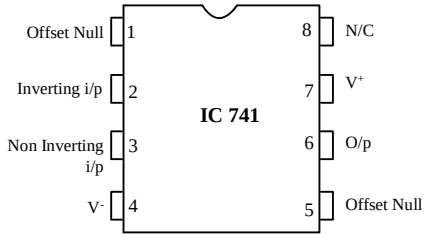
Aim:

To design Inverting, Non-inverting amplifiersusing op-amp and test its performance.

Apparatus required:

S.No	Components	Range	Quantity
1.	Op-amp	IC 741	1
2.	Dual power supply	(0-30) V	1
3.	Function Generator	(0-1) MHz	1
4.	Resistors	10 KΩ, 20 KΩ	2 1
5.	Capacitors	-	-
6	CRO	(0-30) MHz	1

Pin Diagram of IC 741

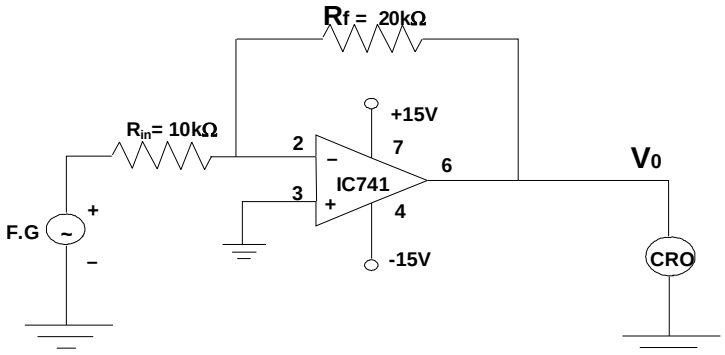


a)Inverting amplifier:[Closed Loop Configuration]

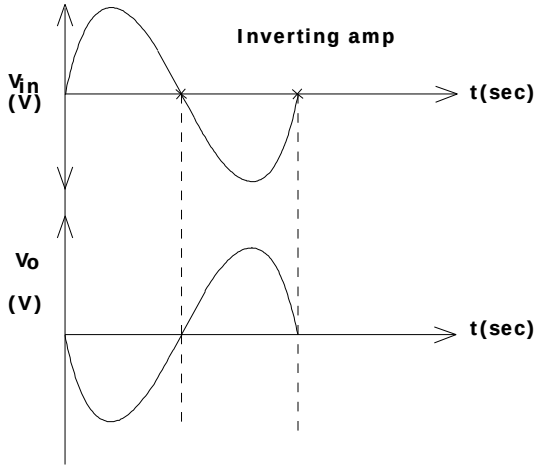
Design:

$A_{CL} = V_o/V_{in} = - R_f/ R_{in}$;
Assume $A_{CL}=2$
$\Rightarrow - R_f/ R_{in}=-2$
Now AssumeR_f= 20kΩ; $\Rightarrow R_{in}$= 10kΩ

Circuit Diagram:



Model Graph:



b) <u>Non inverting amplifier</u>: [Closed Loop Configuration]

<u>Design</u>:

$A_{CL} = V_o / V_{in} = 1 + R_f / R_{in;}$

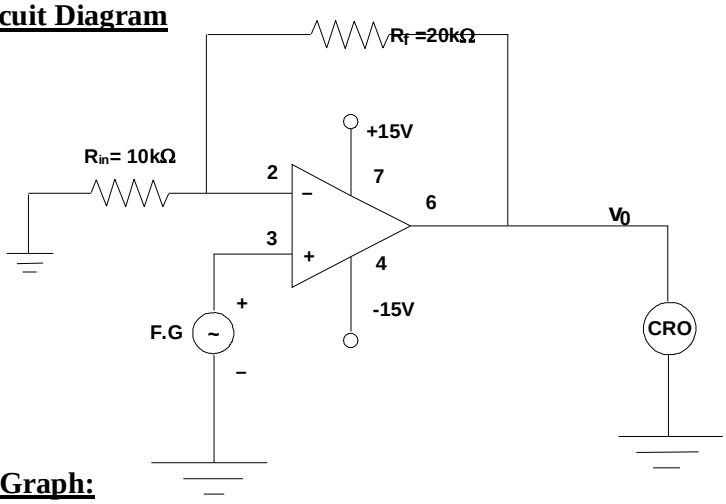
Assume $A_{CL} = 3$;

$\Rightarrow 3 = 1 + R_f / R_{in}$

Assume $R_f = 20k\Omega$;

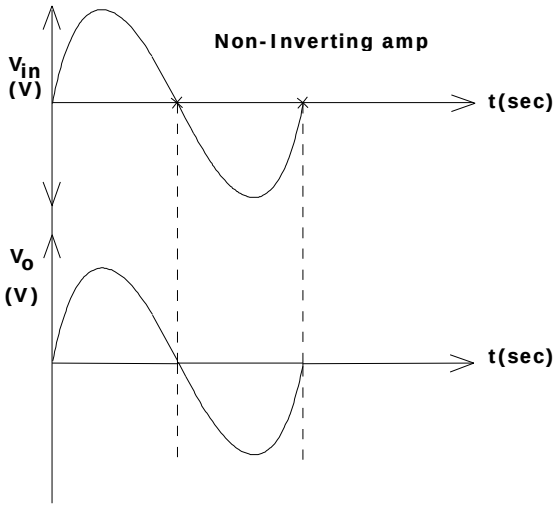
$\Rightarrow R_{in} = 10k\Omega$

<u>Circuit Diagram</u>



<u>Model Graph:</u>

Inverting amplifier:



S.No.	V_{in} (V)	Vo (V)	Practical gain= V_o / V_{in}	Theoretical gain= -(R_f / R_{in})

Non-Inverting amplifier:

S.No.	V_{in} (V)	Vo (V)	Practical gain= V_o / V_{in}	Theoretical gain = 1+(R_f / R_{in})

INVERTING AMPLIFIER:

It is the most widely used of all the op-amp circuits. The output voltage V_o is fed back to the inverting input terminal through the R_f – R_1 network where $R_f$is the feedback resistor. Input signal V_i is applied to the inverting input terminal through R_1 and non-inverting terminal of op-amp is grounded. The gain of the inverting amplifier is given by,

$A_{CL} = V_o/V_i = - R_f/R_1$

The negative sign indicates a phase shift of 180^o between V_i and V_o. The value of R_1 should

be kept large to avoid loading effect.

NON-INVERTING AMPLIFIER:

If the signal is applied to the non-inverting input terminal and feedback is given to the inverting input terminal, the circuit amplifies without inverting the input signal. Such a circuit is called non-inverting amplifier. It is also a negative feedback system as output is being fed back to the inverting input terminal. The gain of non-inverting amplifier is given by,

$$A_{CL} = V_o / V_i = 1 + R_f / R_1$$

The gain can be adjusted to unity (or) more, by proper selection of resistors R_f and R_1. Compared to inverting amplifier, the input resistance of the non-inverting amplifier is extremely large as the op-amp draws negligible current from the signal source.

PROCEDURE:

(i) The circuit connections are given as per the circuit diagram.
(ii) The power supply is switched ON.
(iii) The amplitude and time period of the input and output waveforms are noted from CRO.
(iv) The graph is plotted for the values which will be taken from the CRO.

Result:

Thus Inverting andNon-inverting amplifier using op-amp was designed and tested and the output waveforms are obtained.

EX.No:2

Date:

DESIGN AND TESTING OF INTEGRATOR AND DIFFERENTIATOR

Aim:

To design Integrator and Differentiatorusing op-amp and test its performance.

Apparatus required:

S.No	Components	Range	Quantity
1.	Op-amp	IC 741	1
2.	Dual power supply	(0-30) V	1
3.	Function Generator	(0-1) MHz	1
4.	Resistors	10 kΩ, 100 kΩ 1.5 kΩ, 15 kΩ	2 1 1
5.	Capacitors	0.01 µF, 0.1 µF	1
6	CRO	(0-30) MHz	1

a) Differentiator:

Design:

Step1: Select f_a equal to the highest frequency of the input signal to be differentiated. Then assuming a value of $C_1 < 1\mu F$. Calculate the value of R_f.

Step2: Choose $f_b = 10\ f_a$ and calculate the values of R_1 and C_f so that $R_1C_1 = R_f\ C_f$.

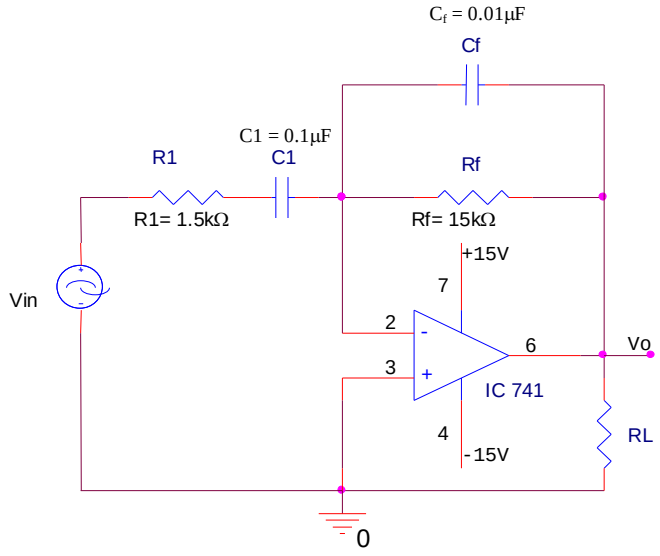
f_a= 1KHz ; f_b =10 KHz ;C_1 = 0.1 µf; $R_{COMP} = R_1$;

$f_a = 1/ [2\pi R_f C_1]$; $R_f = 1/2\pi\ C_1 f_a$;

$f_b = 1/ [2\pi R_1 C_1]$;$R_1 = 1/2\pi\ C_1 f_b$;

$R_1C_1 = R_fC_f$;$C_f = R_1C_1/ R_f$ = 0.01 µF;

Circuit Diagram for Differentiator



Observation:

For sine wave input:

Peak to peak amplitude of the input = volts.

Time Period of the input = ms

Peak to peak amplitude of the output = volts.

Time Period of the output = ms

For square wave input:

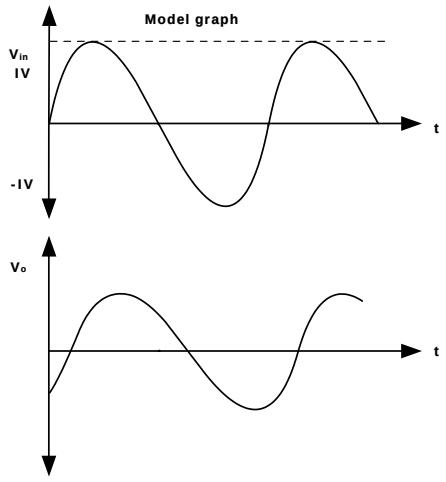
Peak to peak amplitude of the input = volts.

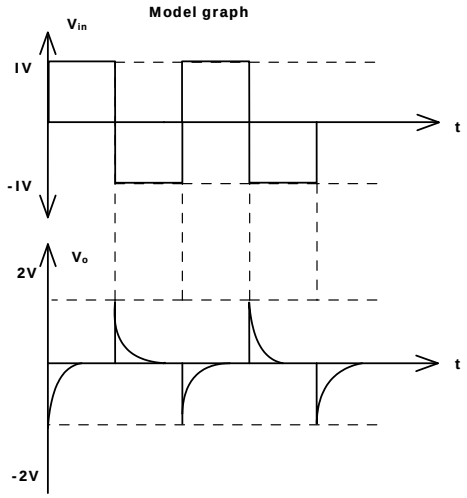
Time Period of the input = ms

Peak to peak amplitude of the output = volts.

Time Period of the output = ms.

Model Graph:





b) Integrator:

Design:

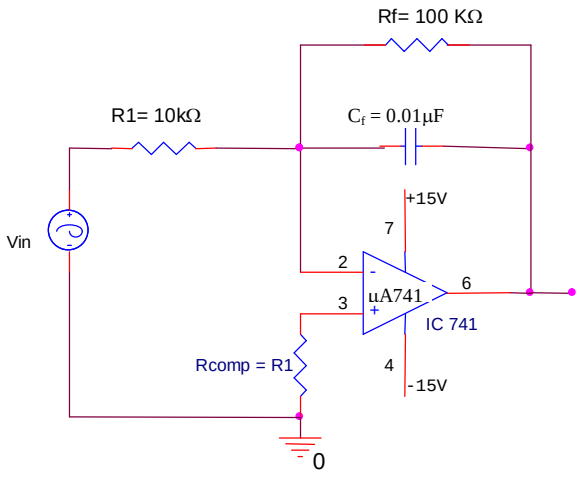
Generally the value of the f_a and in turn R_1C_f and R_fC_f values should be selected such that $f_a<f_b$. From the frequency response we can observe that f_a is the frequency at which the gain is 0 db and f_b is the frequency at which the gain is limited.Maximum input signal frequency = 1 KHz.

Condition is time period of the input signal is larger than or equal to R_fC_f (i.e.) $T \geq R_1C_f$

f_b = 10 KHz ; $f_a = f_b/10$; $R_f = 10R_1$; $R_{COMP} = R_1;R_1 = 10K\Omega$

$f_a = 1/ [2\pi R_fC_f]$; $RfC_f = 0.1msec;Cf = 0.1\ \mu F$

Circuit Diagram for Integrator



$V_O = - [1/R_1C_f] \int Vin\ dt$

Observation:

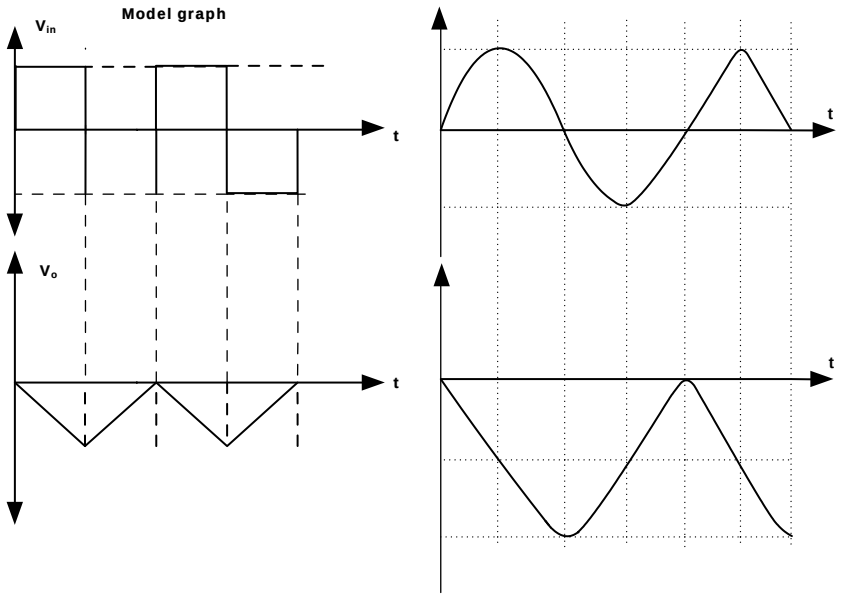
For sine wave input:

Peak to peak amplitude of the input = volts.
Time Period of the input = ms
Peak to peak amplitude of the output = volts.
Time Period of the output = ms

For square wave input:

Peak to peak amplitude of the input = volts.
Time Period of the input = ms
Peak to peak amplitude of the output = volts.
Time Period of the output = ms

Model Graph:



Theory:

DIFFERENTIATOR:

As the name suggests, the circuit performs the mathematical operation of differentiation. That is the output waveform is the derivation of input waveform. The gain of the differentiator increases with increase in frequency which makes the circuit unstable. The output voltage is

$V_o = -R_fC_1(dV_i/dt)$.

The op-amp differentiator is useful for signal wave shaping. The op-amp circuits that contain capacitor is the differentiating amplifier (or) differentiator. A practical differentiator eliminates the problem of stability and high frequency noise. For good differentiation, one must ensure that the time period T of the input signal is larger than (or) equal to R_fC_1, that is,

$T \geq R_fC_1$.

The expression of the output voltage remains same as in the case of an ideal differentiator.

INTEGRATOR:

The op-amp integrator is useful for signal wave shaping. If we interchange the resistor and capacitor of the differentiator, we have the circuit of an integrator. A simple RC circuit can also work as an integrator when time constant is very large. This requires very large values of R and C. The components R and C cannot be made infinitely large because of practical limitations. Thus integrator circuit does not have any high frequency problem unlike a differentiator circuit. However, at low frequencies such as at dc, the gain becomes infinite.

The op-amp saturates, i.e., the capacitor is fully charged and it behaves like an open circuit. The gain of an integrator at low frequency can be limited to avoid the saturation problem if the feedback capacitor is shunted by a resistance R_f. The parallel combination of R_f and $C_f$behaves like a practical capacitor which dissipates power unlike an ideal capacitor For this reason, this circuit is also called a lossy integrator. The resistor R_f limits the low frequency gain to R_f/R_1 and thus provides dc stabilization. The output voltage is expressed as,

$V_o(t) = -1/R_1C_f \int V_i(t)\, dt + V_o(0)$.

$V_o = -1/R_1C_f \int V_i dt$.

Where $V_o(0)$ is the initial output voltage. Thus the output is $-1/R_1C_f$ times the integral of input and R_1C_f is the time constant of the integrator.

PROCEDURE:

(i) The circuit connections are given as per the circuit diagram.

(ii) The power supply is switched ON.

(iii) The amplitude and time period of the input and output waveforms are noted from
CRO.

(iv) The graph is plotted for the values which will be taken from the CRO.

Result:

Thus Integrator and Differentiator using op-amp was designed and tested and the output waveforms are obtained.

Ex.No:3
Date:

SUMMER,SUBTRACTOR USING OP-AMP

AIM:
To design summer and subtractor using operational amplifier 741 and test the operation.

APPARATUS REQUIRED:

S.NO	COMPONENTS	RANGE	QUANTITY
1	IC741		1
2	Function Generator	3MHZ	2
3	CRO	30MHZ	1
4	Dual Power Supply	±12V	1
5	Resistors	1KΩ, 2KΩ	6 1

DESIGN:
ADDER:

Assume $R_1 = R_2 = R_F = 1K\Omega$

$V_o = -((R_F/R_1)V_1+(R_F/R_2)V_2$
$= -(V_1+V_2)$ Volts

DIFFERENCE AMPLIFIER:

$V_o = R_2/R_1(V_1 - V_2)$

Put $R_2 = 1K\Omega$, $R_1 = 1K\Omega$.

Then $V_o = V_1 - V_2$.

THEORY:

ADDER:
An inverting Summing Amplifier amplifies the linear summation of input signals.

$I=V_1/R_1+V_2/R_2 \ldots\ldots. V_N/R_N$

$V_o = -R_F I$

$= -((R_F/R_1)V_1+(R_F/R_2)V_2\ldots\ldots.(R_F/R_N)V_N)$.

If $R_F=R_1=R_2\ldots\ldots=R_N$, then $V_0= -(V_1+V_2+\ldots..+V_N)$.

The Op-amp in non-linear inverting mode can be used to produce an output that is linear combination of inputs without sign change.

DIFFERENCE AMPLIFIER:
A circuit that amplifies the difference between two signals is called a difference amplifier. This type of the amplifier is very useful in instrumentation

circuits. The output voltage of the difference amplifier is given by,

$V_o = R_2 / R_1 (V_1 – V_2)$

Such a circuit is very useful in detecting very small differences in signals, since the gain R_2 / R_1 can be chosen to be very large.

If $R_2 = R_1$, $V_o = V_1 – V_2$;

TABULATION:

ADDER

S.No	V_1	V_2	$V_0=-(V_1+V_2)$
1.			
2.			

SUBTRACTOR

S.No	V_1	V_2	$V0=V_1-V_2$
1.			
2.			

PROCEDURE:

(i) The circuit connections are given as per the circuit diagram.

(ii) The power supply is switched ON.

(iii) The amplitude and time period of the input and output waveforms are noted from CRO.

(iv) The graph is plotted for the values which will be taken from the CRO.

RESULT:

Thus adder and subtractor circuits were designed using operational amplifier IC 741 and tested.

Ex.No:4

Date:

DESIGN OF TRIANGULAR WAVE GENERATOR USING IC 741

Aim:

To design a Triangular Wave Generator with a specified frequency.

Components Required:

S.No	Components	Range	Quantity
1.	Op-amp	IC 741	2
2.	Dual power supply	(0-30) V	1
3.	Resistors	100KΩ 10 KΩ 20 KΩ	1 1 1
4.	Capacitors	0.01 µF	1
5.	CRO	(0-30) MHz	1
6.	Probes	--	1

DESIGN:

Let ±Vsat = ± 14 V.

Frequency of oscillation fo=500 Hz.

Time period , $T=(4R_1C_1R_2)/ R_3$.

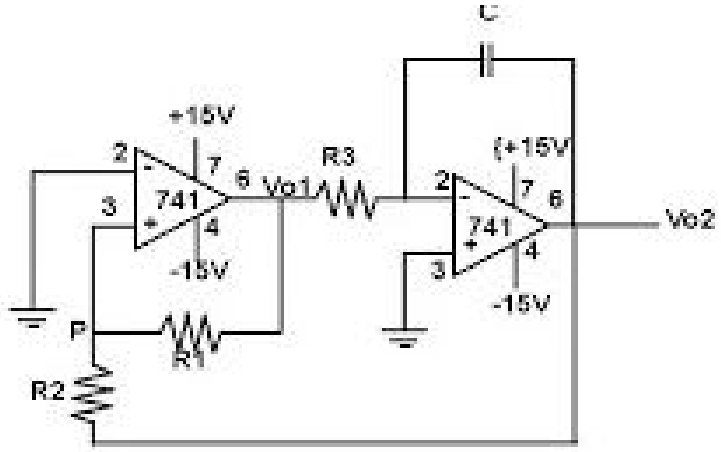
Assume R_1= 100 KΩ, R_2 =10K Ω C_1= 0.01 µF.

Then $R_3=(4 R_1C_1R_2)/T$ = 20 K Ω.

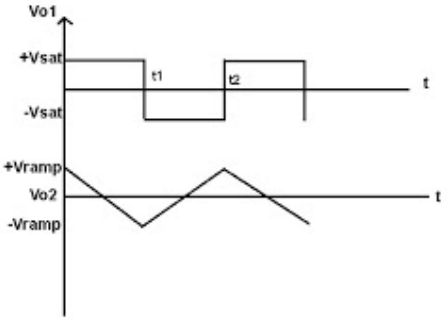
TABULATION:

AMPLITUDE(v)	TIME PERIOD (ms)	PRACTICAL FREQUENCY(KHz)	THEORITICAL FREQUENCY (KHZ)

CIRCUIT DIAGRAM:



MODEL GRAPH:



THEORY:

This is the circuit for Triangular wave generator using 741 op amp. The integrator output waveform will be triangular if the input to it is a square wave. It means that a triangular wave generator can be formed by simply cascading an integrator and a square wave generator.This circuit uses two operational amplifiers. First op amp functions as a comparator and next op amp as an integrator.

Comparator compares the voltage at a point 'P' continuously with respect to the voltage at the inverting input, which is at ground potential.When the voltage at P goes slightly below zero, the output of comparator will switches to negative saturation.Consider the output of comparator is +Vsat, since this voltage is the input of integrator, then its output will be negative going ramp.Thus one end of the potential divider R1 R2 is at +Vsat and other end is at negative going ramp. When the negative going ramp attains a value say –Vramp the effective voltage at P becomes slightly less than 0V. This switches output of comparator to –Vsat.During this time integrator output will be positive going ramp. When the value of positive going ramp attains +Vramp, voltage at 'P' becomes slightly greater than 0V, there by switching comparator output to +Vsat.This cycle repeats and generates a triangular waveform.

Procedure:

1. Connect the circuits as shown in the circuit

2. Switch on the power supply.
3. Note down the output voltage on the CRO.
4. Plot the output waveforms on the graph.
5. Compare the practical value of the frequency with the theoretical value.

Result:

Thus Triangular Wave Generator is designed using IC 741 and the waveforms are plotted**.**

Ex.NO.:5
Date:

RC PHASE SHIFT OSCILLATORS USING OPERATIONAL AMPLIFIER

Aim:

To design an RC Phase shift oscillator with aspecified frequency.

Components Required:

S.No	Components	Range	Quantity
1.	Op-amp	IC 741	1
2.	Dual power supply	(0-30) V	1
3.	Resistors	435KΩ,10KΩ 15 KΩ 1.5KΩ	1 1 3
4.	Capacitors	0.1 µF	3
5.	CRO	(0-30) MHz	1
6.	Probes	--	1

Design:

Frequency of oscillation fo = $1/(\sqrt{6}*2*\Pi*RC)$

Av = [Rf/R1] = 29

R_1 = 10 R

R_f = 29 R_1

Given fo = 500 Hz.

Let C = 0.1µF

R = $1/(\sqrt{6}*2*\Pi*fo*C)$

= 1.5 KΩ.

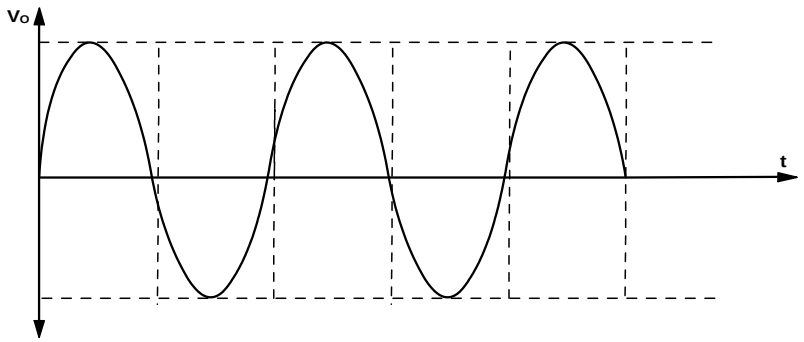
To prevent loading of amplifier by RC network, R1≥10R,

R1 = 15 KΩ.

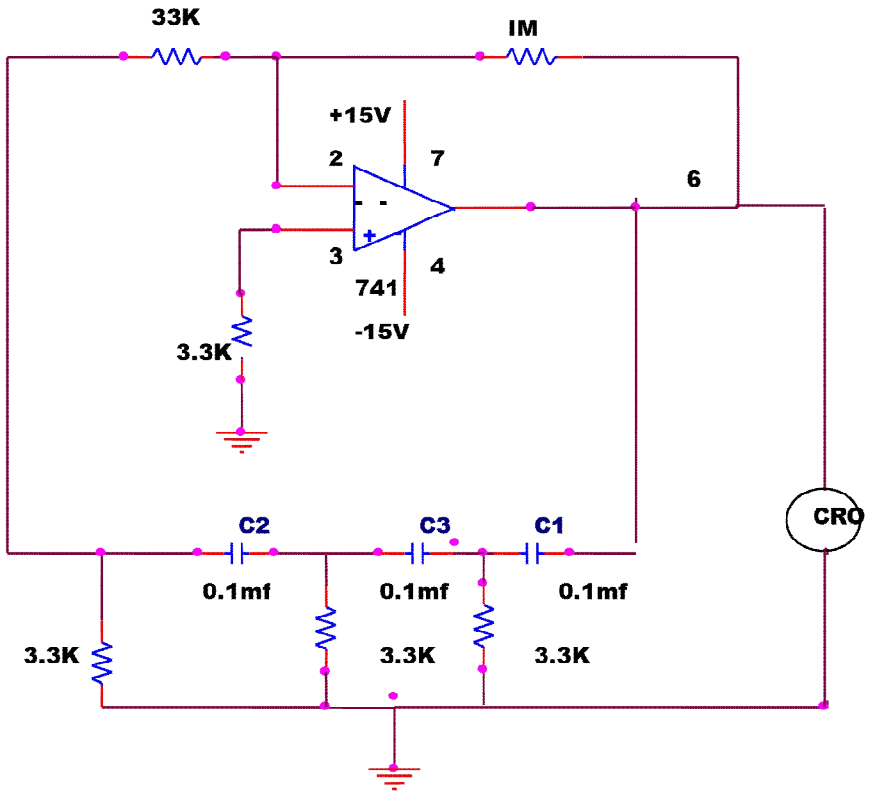
SinceRf=29 R1,

Rf = 435 KΩ.

Model Graph:



Circuit Diagram



TABULATION:

AMPLITUDE(v)	TIME PERIOD (ms)	PRACTICAL FREQUENCY(KHz)	THEORITICAL FREQUENCY (KHZ)

THEORY:

A phase shift oscillator, which consists of an op-amp as the amplifying stage and three RC cascaded networks as the feedback circuit that provides feedback voltage from the output back to the input of the amplifier. The op-amp is used in the inverting mode. Therefore, any signal that appears at the inverting terminal is shifted by 180^o phase shift required for oscillation. Thus the total phase shift around the loop is 360^o. The frequency of oscillation f_o if this phase shift oscillator is given by

$$f = 1 / (2\pi\sqrt{(6)}\, RC).$$

Procedure:

1. Connect the circuits as shown in the circuit
2. Switch on the power supply.
3. Note down the output voltage on the CRO.
4. Plot the output waveforms on the graph.
5. Compare the practical value of the frequency with the theoretical value.

Result:

Thus RC Phase shift oscillator was designed using op-amp and tested and its frequency is determined.

Ex.No:6

Date:

DESIGN AND TESTING OF SCHMITT TRIGGER USING OP-AMP

Aim:

To design a Schmitt trigger using op-amp and test its performance.

Apparatus required:

S.No	Components	Range	Quantity
1.	Op-amp	IC 741	1
2.	Dual power supply	(0-30) V	1
3.	Function Generator	(0-1) MHz	1
4.	Resistors	1 kΩ, 4 kΩ	1 1
5.	CRO	(0-30) MHz	1

Schmitt Trigger:

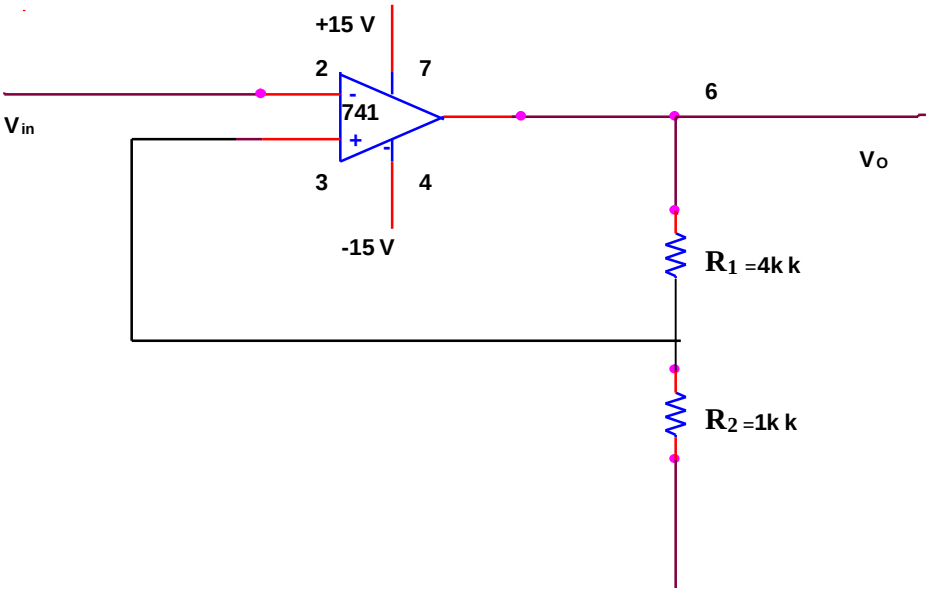
Design

V_{CC} = 12 V; V_{SAT} = 0.9 V_{CC}; R1= 4KΩ; R2 = 1KΩ

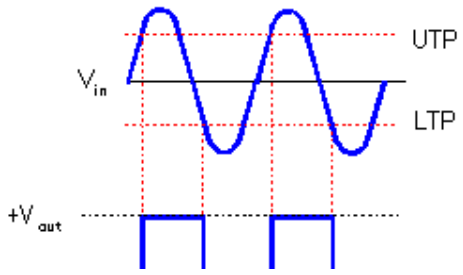
V_{UT} = + [V_{SAT} R_2] / [R_1+R_2] & V_{LT} = - [V_{SAT} R_2] / [R_1+R_2]

HYSTERSIS [H] = V_{UT} - V_{LT}

Circuit Diagram



Model Graph



Observation:

Peak to peak amplitude of the output = Volts.

Time period of the output = ms.

Upper threshold voltage = Volts.

Lower threshold voltage = Volts.

Theory:

The Schmitt Trigger is also known as Regenerative Comparator. If positive feedback is added to the comparator circuit, gain can be increased greatly. The transfer curve of comparator becomes more close to ideal curve. Theoretically, if the loop gain – βA_{OL} is adjusted to unity, then the gain with feedback, A_{Vf} becomes infinite. This result in an abrupt transition between the extreme values of output voltage. In practical circuits, it may not be possible to maintain loop-gain exactly equal to unity for a long time because of supply voltage and temperature variations. So a value greater than unity is chosen. This also gives an output waveform virtually discontinuous at the comparison voltage. This circuit exhibits a phenomenon called hysteresis (or) backlash. As long as input voltage is less than upper threshold voltage VUT, output voltage remains constant at +Vsat.

For $V_i > V_{UT}$; V_O= -Vsat.

As long as input voltage is greater than lower threshold voltage VUT, output voltage remains constant at -Vsat.

For $V_i > V_{LT}$; V_O= +Vsat.

Procedure

1. Connect the circuit as shown in the circuit
2. Set the input voltage as 5V (p-p) at 1KHz. (Input should be always less than V_{cc})
3. Note down the output voltage at CRO
4. To observe the phase difference between the input and the output, set the CRO in dual Mode and switch the trigger source in CRO to CH1.
5. Plot the input and output waveforms on the graph.

Result:

Thus Schimitt triggeris designed using op-amp and the waveforms are plotted.

Ex No:7
Date:

ACTIVE LOW PASS AND HIGH PASS FILTERS

Aim:-

To design and test the frequency response of a second order LPF and HPF.

Components Required:-

S.No	Components	Range	Quantity
1.	Op-amp	IC 741	3
2.	Resistors		
3.	Capacitor	O.01μf, O.05μf	2
4.	CRO		1
5.	Power Supply	± 15V	1
6.	Probe		2
7.	Bread Board		1

Theory:-

BSF:-

BSF is the logical inverse of band pass filter which does not allows a specified range of frequencies to pass through. It has two pass bands in the range of frequencies between 0 to f_L and beyond f_H. The band between f_L and f_H is called stop band. BSF is also called Band Reject Filter (BRF) or Band Elimination Filter (BEF).

BPF:-

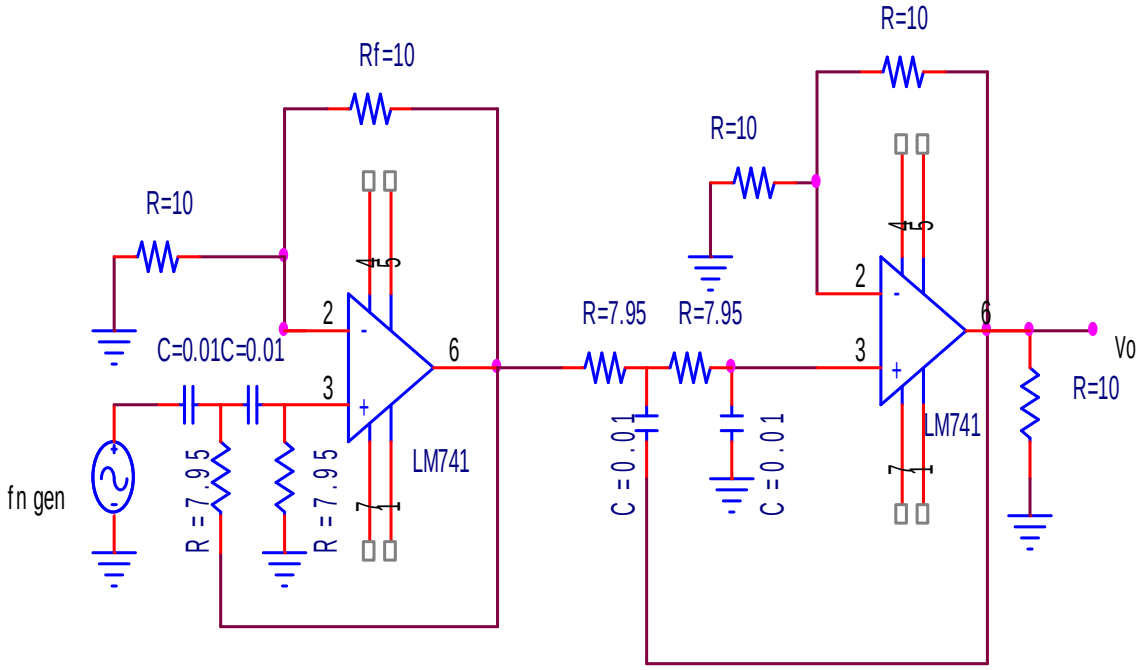
The BPF is the combination of high and low pass filters and this allows a specified range of frequencies to pass through. It has two stop bands in range of frequencies between 0 to f_L and beyond f_H. The band b/w f_L and f_H is called pass band. Hence its bandwidth is (f_L-f_H). This filter has a maximum gain at the resonant frequency (f_r) which is defined as

$$f_r = \sqrt{f_H f_L}$$

The figure of merit (or) quality factor Q is given by

$$Q = \frac{f_r}{f_H - f_L} = \frac{f_r}{BW}$$

Circuit Diagram:-
BPF



Design:-
BSF:-

f_H=200Hz
f_L=1kHz

Low pass section:-

f_H=200Hz
Let C^1=0.05μf
Then,

$$R^1 = \frac{1}{2\pi f_H c^1}$$

$$R^1 = \frac{1}{2\pi\,(200\,)(\,0.05 \times 10^{-6})}$$

$$R^1 = 15.9K\Omega$$

$$C^1 = 0.05\ \mu f$$

High Pass Section:-

$$f_L = 1 \text{ KHZ}$$

$$C = 0.01 \ \mu f$$

$$R = \frac{1}{2\pi f_L C}$$

$$= \frac{1}{2\pi (1 \times 10^{3})(0.01 \times 10^{-6})}$$

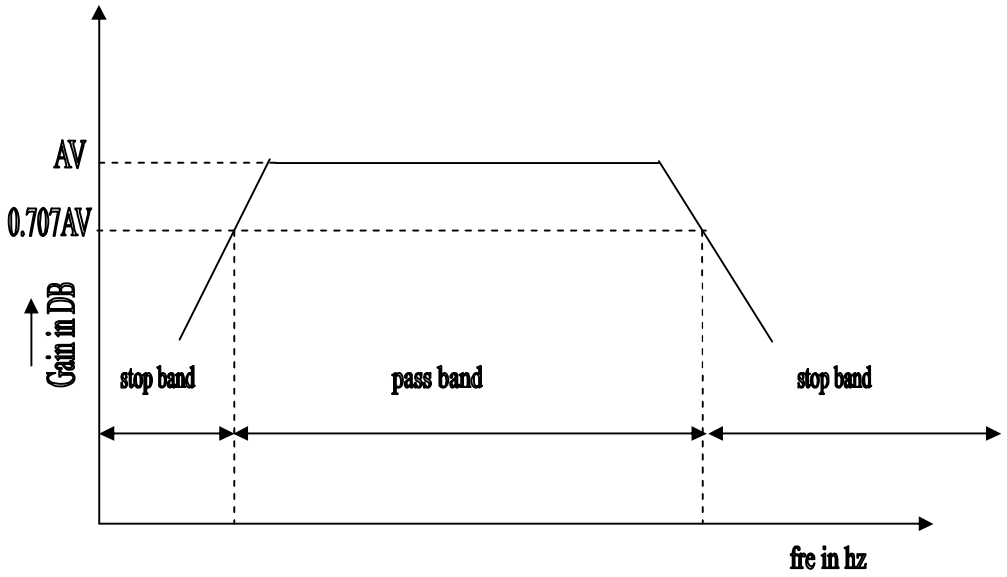
$$R = 15.9 \text{ K}\Omega$$

Gain, Av=2 for each section

$$\therefore R_1 = R_f = R_1^1 = R_f^1 = 10 \text{ K}\Omega$$

Model graph:-

BPF:-



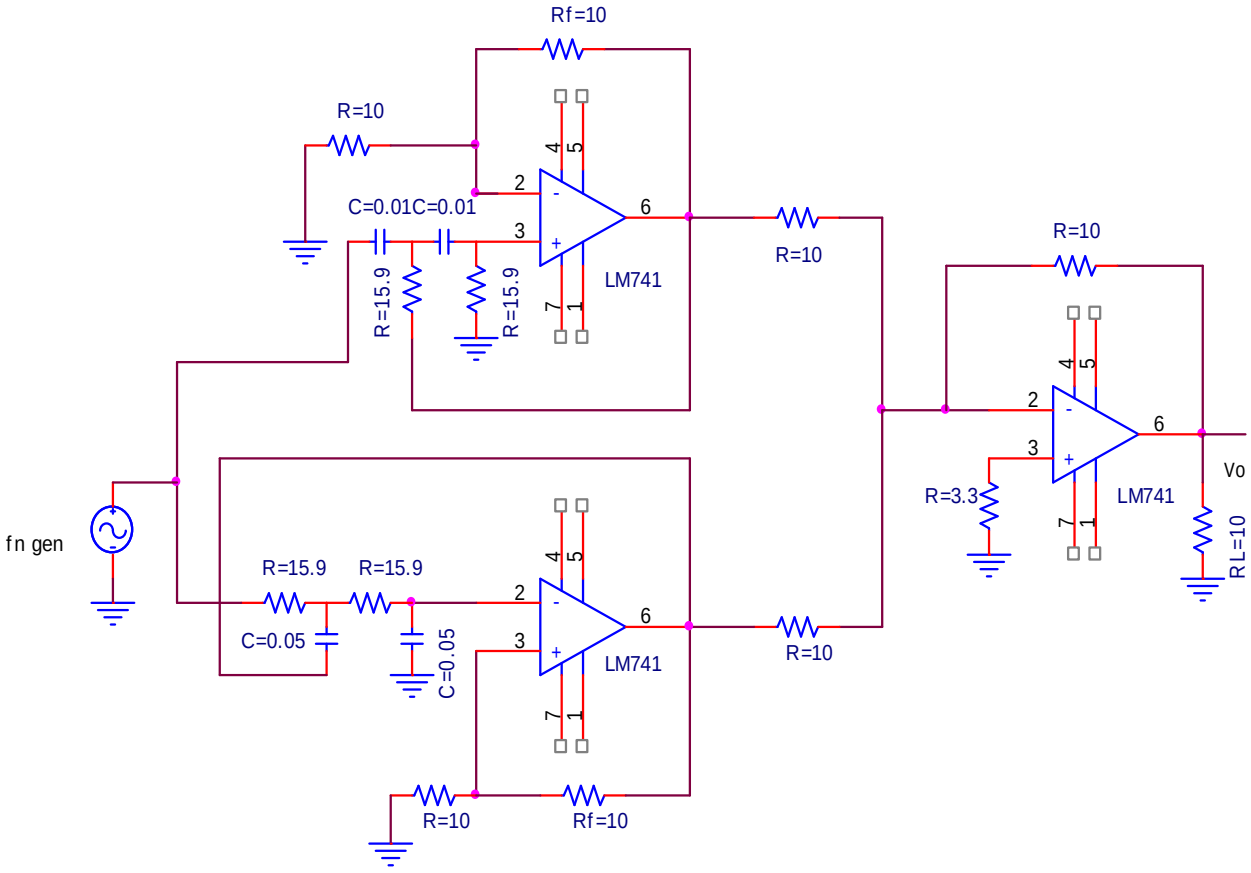
Tabulation:-

BPF Vin=50mv

S.No	Frequency (Hz)	Vo(volts)	Gain=20log(Vo/Vin)

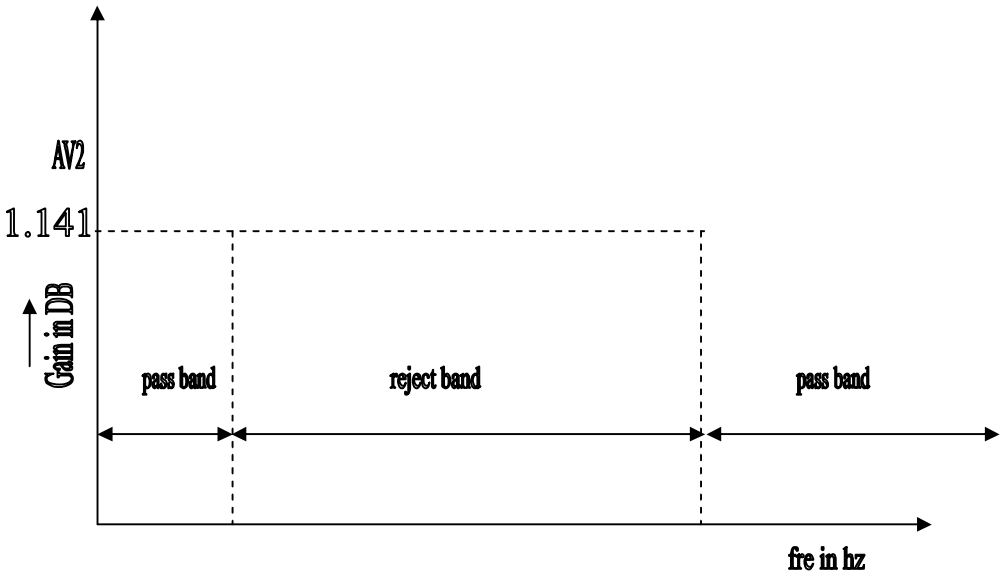
Circuit Diagram:-

BSF



Model graph:-

BSF:-



Tabulation:-

BSF

Vin=50mv

S.No	Frequency (Hz)	Vo(volts)	Gain=20log(Vo/Vin)

Procedure:

BSF,BPF:-

1. The input signal is connected to the circuit from the signal generator.
2. The input and output signals are connected to the filter.
3. The suitable voltage is selected.
4. The correct polarity is checked.
5. The steps are repeated.

Result:-

Thus the frequency response of second order BPF and BSF filter was designed and tested.

Ex.NO: 8

Date:

ASTABLE MULTIVIBRATOR USING IC555

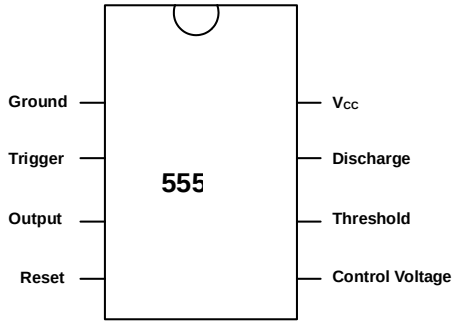
Aim:

To design and test an Astable Multivibrators using 555 timer.

Apparatus Required:

S.No	Component	Range	Quantity
1.	555 TIMER		1
2.	Resistors	10KΩ, 12KΩ	1
3.	Capacitors	0.01μ F	2
5.	CRO		1
6.	Power supply	+ 5 V	1
7.	Probe		2
8.	Bread Board		1

Pin diagram:



DESIGN:

fo =1/T = 4 KHZ

Choosing C = 0.01 μF;

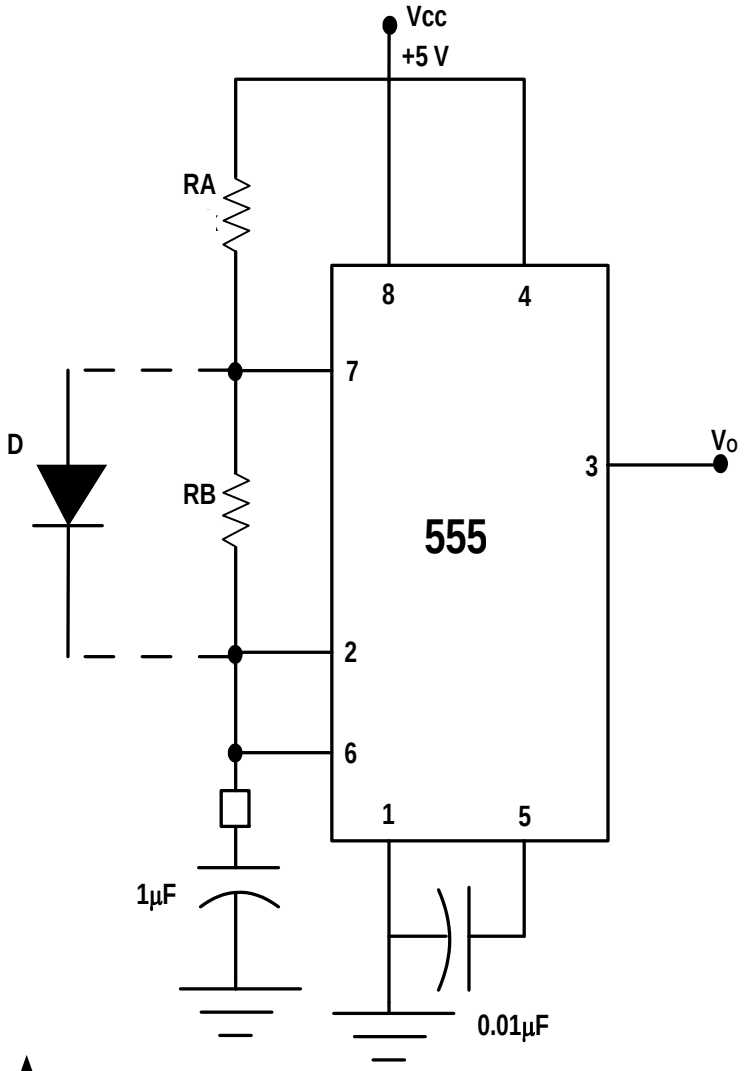
R_A = 10 KΩ

Assume duty cycle = 65%

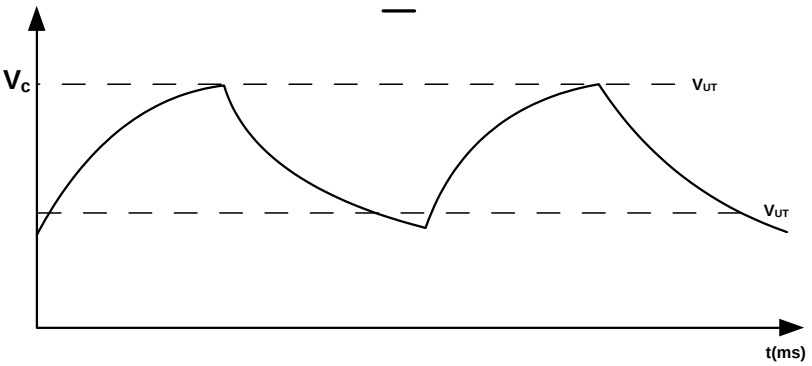
Duty cycle = Tc/(Tc + Td) = 0.65

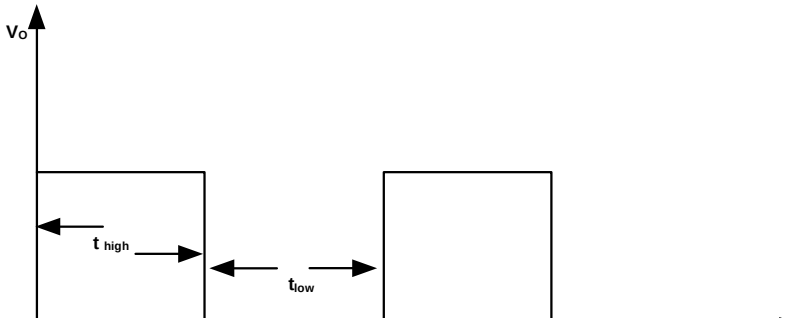
R_B = Td/(0.693 C) =12 KΩ

Circuit Diagram



Model Graph





AstableMultivibrators using 555

Fig shows the 555 timer connected as an AstableMultivibrators. Initially, when the output is high. Capacitor C starts charging towards V_{cc} through R_A and R_B. As soon as capacitor voltage equals 2/3 V_{cc} upper comparator (UC) triggers the flip flop and the output switches low. Now capacitor C starts discharging through R_B and transistor Q_1.

When the voltage across C equals 1/3 V_{cc} lower comparator (LC), output triggers the flip-flop and the output goes high. Then the cycle repeats.

The capacitor is periodically charged and discharged between 2/3 $V_{cc}$and 1/3 V_{cc}respectively. The time during which the capacitor charges form 1/3 V_{cc} to 2/3 V_{cc} is equal to the time the output is high and is given by

$$T_c = 0.69(R_A+R_B)C \quad (1)$$

Where R_A and R_B are in Ohms and C is in farads. Similarly the time during which the capacitor discharges from 2/3 V_{cc} to 1/3 $V_{cc}$is equal to the time the output is low and is given by

$$T_d = 0.69\ R_BC \quad (2)$$

The total period of the output waveform is

$$\mathbf{T = T_c + T_d = 0.69\ (R_A + 2R_B)\ C} \quad (3)$$

The frequency of oscillation

$$f_o = 1 / T = 1.45 / (R_A+2R_B)C \quad (4)$$

Procedure:

1. Rig-up the circuit of 555 AstableMultivibrators as shown in fig with the designed value of components.
2. Connect the CRO probes to pin 3 and 2 to display the output signal and the voltage across the timing capacitor. Set suitable voltage sensitively and time-base on the CRO.
3. Switch on the power supply to CRO and the circuit.
4. Observe the waveforms on the CRO and draw to scale on a graph sheet. Measure the voltage levels at which the capacitor starts charging and discharging, output high and low timings and frequency.
5. Observe the output waveform. Draw to scale on a graph sheet.

Result:

Thus AstableMultivibrator is designed using 555 Timer and the waveforms are plotted.

Ex.NO:9

Date:

MONOSTABLE MULTIVIBRATOR USING IC555

Aim:

To design and test an Monostable Multivibrators using 555 timer .

Apparatus Required:

S.No	Component	Range	Quantity
1.	555 TIMER		1
2.	Resistors	10K, 6.8k	1
3.	Capacitors	0.1 μ F, 0.01μ F	2
5.	CRO		1
6.	Power supply	± 15 V	1
7.	Probe		2
8.	Bread Board		1

Design:

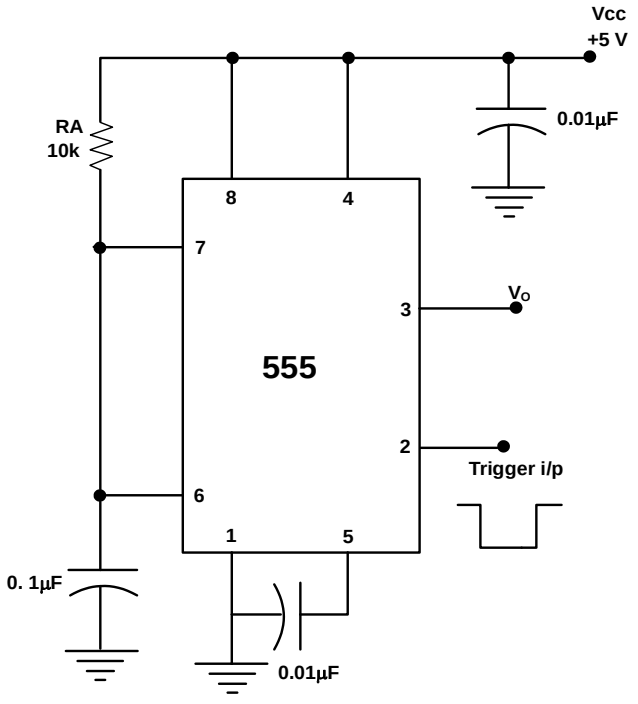
Let C = 0.01 μf; Here, T= 1.1 R_AC;

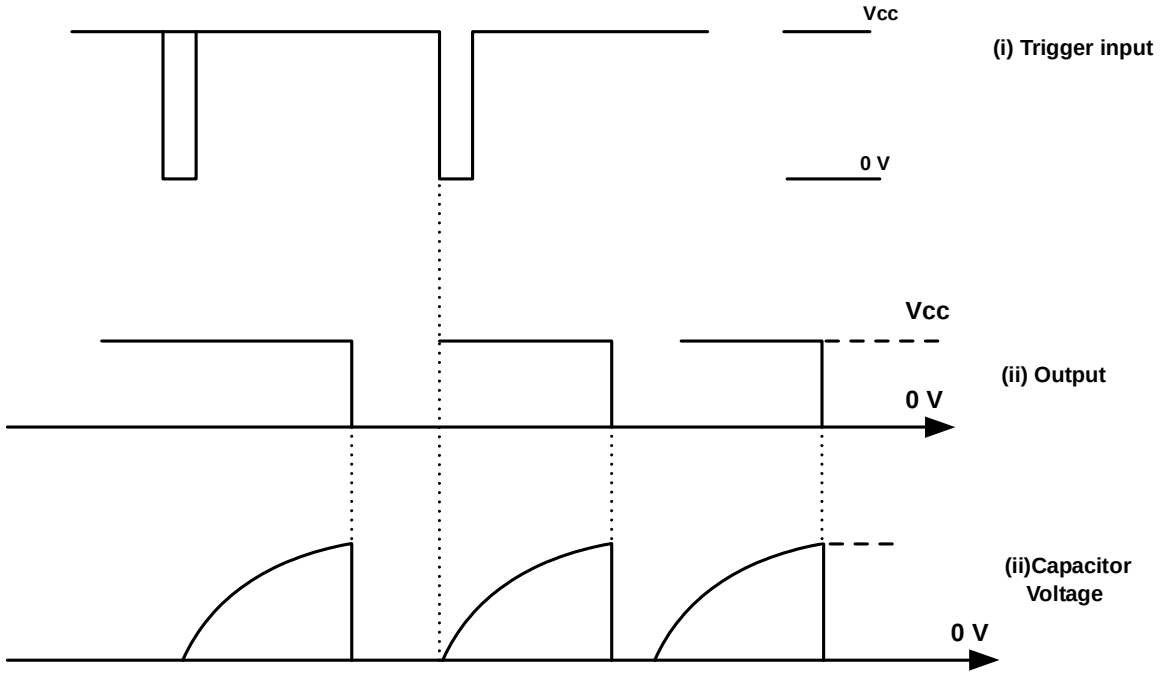
T is designed for a value of 0.11ms.

So, R_A = T/(1.1 C) =10 KΩ.

Circuit Diagram

Model Diagram:





Theory:

Monostable Multivibrators using 555

Monostable Multivibrators has one stable state and other is a quasi stable state. The circuit is useful for generating single output pulse at adjustable time duration in response to a triggering signal. The width of the output pulse depends only on external components, resistor and a capacitor.

The stable state is the output low and quasi stable state is the output high. In the stable state transistor Q1 is 'on' and capacitor C is shorted out to ground. However upon application of a negative trigger pulse to pin2, Q1 is turned 'off' which releases the short circuit across the external capacitor C and drives the output high. The capacitor C now starts charging up towards V_{cc} through R_A. However when the voltage across C equal 2/3 V_{cc} the upper comparator output switches form low to high which in turn drives the output to its low state via the output of the flip flop. At the same time the output of the flip flop turns Q1 'on' and hence C rapidly discharges through the transistor. The output remains low until a trigger is again applied. Then the cycle repeats.

The pulse width of the trigger input must be smaller than the expected pulse width of the output. The trigger pulse must be of negative going signal with amplitude larger than 1/3 Vcc. The width of the output pulse is given by,

$$T = 1.1\ R_A C$$

Procedure:

1. Rig-up the circuit of 555 monostable Multivibrators as shown in fig with the designed value of components.
2. Connect the trigger input to pin 2 of 555 timer form the function generator.
3. Connect the CRO probes to pin 3 and 2 to display the output signal and the voltage across the timing capacitor. Set suitable voltage sensitively and time-base on the CRO.
4. Switch on the power supply to CRO and the circuit.
5. Observe the waveforms on the CRO and draw to scale on a graph sheet. Measure the voltage levels at which the capacitor starts charging and discharging, output high and low timings along with trigger pulse.

Result:

Thus the Monostable Multivibrators using 555 timer is designed and tested.

Ex.No:10
Date:

DESIGN OF SCHMITT TRIGGER USING 555 TIMER

Aim:

To design a Schmitt trigger using op-amp and test its performance.

Apparatus required:

S.No	Components	Range	Quantity
1.	Timer	IC 555	1
2.	Power supply	+ 5 V	1
3.	Function Generator	(0-1) MHz	1
4.	Resistors	10 kΩ, 12 kΩ	1 1
5.	CRO	(0-30) MHz	1
6.	Capacitors	0.1 µF,0.01 µF	1

THEORY:

The Schmitt Trigger is also known as Regenerative Comparator. If positive feedback is added to the comparator circuit, gain can be increased greatly.Fig shows the 555 timer connected as anSchmitt Trigger. Initially, when the output is high. Capacitor C starts charging towards V_{cc} through $R_1$and R_2. As soon as capacitor voltage equals 2/3 V_{cc} upper comparator (UC) triggers the flip flop and the output switches low. Now capacitor C starts discharging .When the voltage across C equals 1/3 V_{cc} lower comparator (LC), output triggers the flip-flop and the output goes high. Then the cycle repeats.

The capacitor is periodically charged and discharged between 2/3 $V_{cc}$and 1/3 V_{cc}respectively. The time during which the capacitor charges form 1/3 V_{cc} to 2/3 V_{cc} is equal to the time the output is high and is given by

$$T_c = 0.69(R_1+R_2)C \quad (1)$$

Similarly the time during which the capacitor discharges from 2/3 V_{cc} to 1/3 $V_{cc}$is equal to the time the output is low and is given by

$$T_d = 0.69\ R_2C \quad (2)$$

The total period of the output waveform is

$$\mathbf{T = T_c + T_d = 0.69\ (R_1 + 2R_2)\ C} \quad (3)$$

The frequency of oscillation

$$f_o = 1 / T = 1.45 / (R_1+2R_2)C \quad (4)$$

As long as input voltage is less than upper threshold voltage VUT, output voltage remains constant at +Vsat. For $V_i > V_{UT}$; V_O= -Vsat.

As long as input voltage is greater than lower threshold voltage VUT, output voltage remains constant at -Vsat. For $V_i > V_{LT}$; V_O= +Vsat.

DESIGN:

fo =1/T = 4 KHZ ; Choosing C = 0.01 μF;

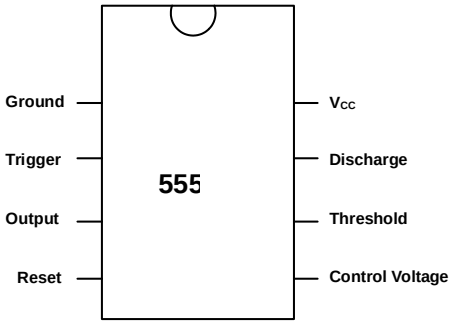
R_1 = 10 KΩ

Assume duty cycle = 65%

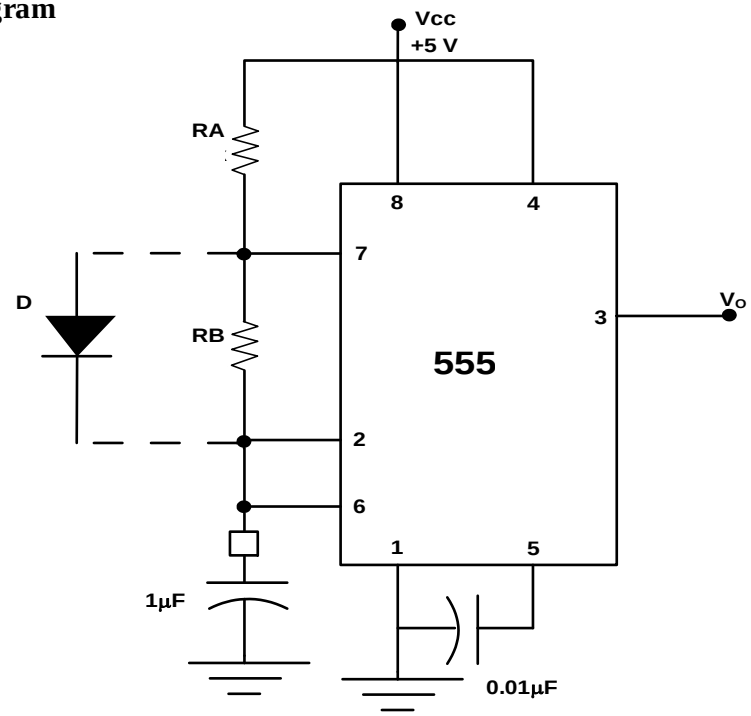
Duty cycle = Tc/(Tc + Td) = 0.65

R_2 = Td/(0.693 C) =12 KΩ

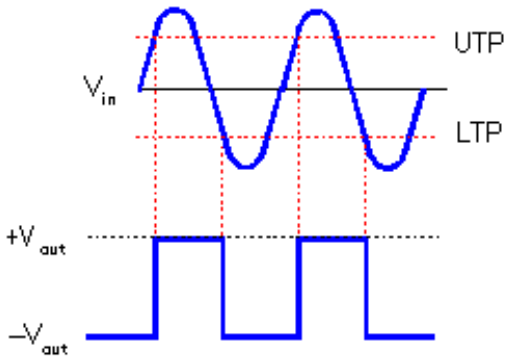
Pin diagram:



Circuit Diagram



Model Graph:



Observation:

Peak to peak amplitude of the output = Volts.

Time period of the output = ms.

Upper threshold voltage = Volts.

Lower threshold voltage = Volts.

Procedure

1. Connect the circuit as shown in the circuit
2. Set the input voltage as 5V (p-p) at 1KHz. (Input should be always less than V_{cc})
3. Note down the output voltage at CRO
4. To observe the phase difference between the input and the output, set the CRO in dual Mode and switch the trigger source in CRO to CH1.
5. Plot the input and output waveforms on the graph.

Result:

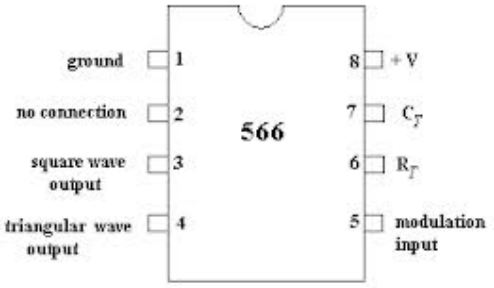
Thus Schimitt trigger is designed using IC 555 and the waveforms are plotted.

Ex.No: 11
Date:

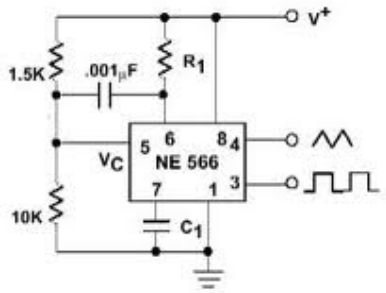
VOLTAGE CONTROLLED OSCILLATOR

Aim:

To design a Voltage Controlled Oscillator



Circuit Diagram:



Theory

A VCO is a circuit that provides an oscillating output signal (typically of square-wave or triangular waveform) whose frequency can be adjusted over a range by a dc voltage. An example of a VCO is the 566 IC unit, that provides simultaneously the square-wave and triangular-wave outputs as a function of input voltage. The frequency of oscillation is set by an external resistor R_1 and a capacitor C_1 and the voltage V_c applied to the control terminals. Figure shows that the 566 IC unit contains current sources to charge and discharge an external capacitor C_v at a rate set by an external resistor R_1 and the modulating dc input voltage. A Schmitt trigger circuit is employed to switch the current sources between charging and discharging the capacitor, and the triangular voltage produced across the capacitor and square-wave from the Schmitt trigger are provided as outputs through buffer amplifiers. Both the output waveforms are buffered so that the output impedance of each is 50 f2. The typical magnitude of the triangular wave and the square wave are 2.4 $\mathbf{V_{peak\cdot to\text{-}peak}}$ **and** $\mathbf{5.4V_{peak\cdot to\cdot peak.}}$

The frequency of the output waveforms is approximated by

$$\mathbf{f_{out} = 2(V^+ - V_c)/R_1C_1V^+}$$

TABULATION:

AMPLITUDE(v)	TIME PERIOD (ms)	PRACTICAL FREQUENCY(KHz)	THEORITICAL FREQUENCY (KHZ)

Procedure:

1. Connect the circuits as shown in the circuit
2. Switch on the power supply.
3. Note down the output voltage on the CRO.
4. Plot the output waveforms on the graph.
5. Compare the practical value of the frequency with the theoretical value

Result:

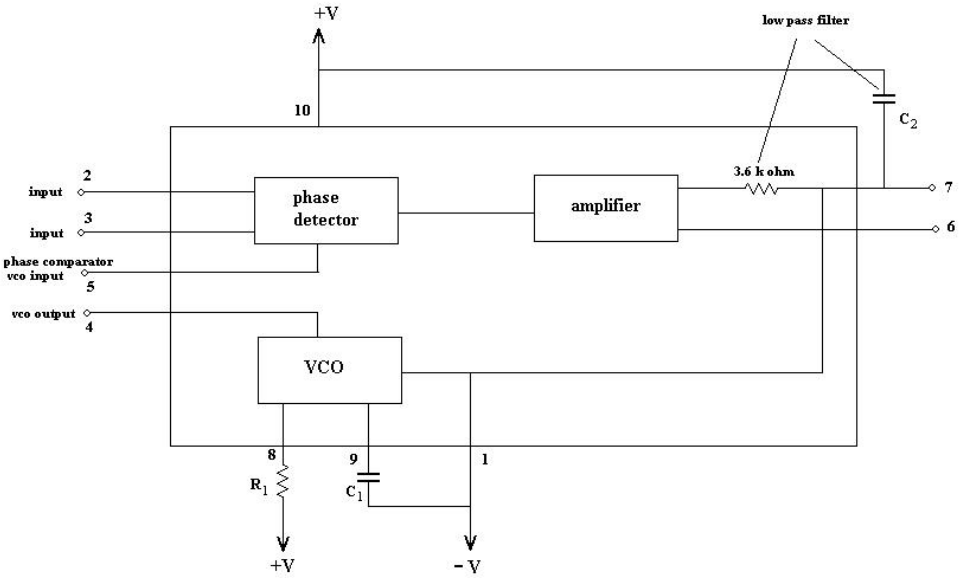
Thus the VCO is designed and the waveforms are plotted.

PLL IC 565

THEORY:-

The Signetics SE/NE 560 series is monolithic phase locked loops. The SE/NE 560, 561, 562, 564, 565, & 567 differ mainly in operating frequency range, power supply requirements and frequency and bandwidth adjustment ranges. The device is available as 14 Pin DIP package and as 10-pin metal can package. Phase comparator or phase detector compare the frequency of input signal f_s with frequency of VCO output f_o and it generates a signal which is function of difference between the phase of input signal and phase of feedback signal which is basically a d.c voltage mixed with high frequency noise. LPF remove high frequency noise voltage. Output is error voltage. If control voltage of VCO is 0, then frequency is center frequency (f_o) and mode is free running mode. Application of control voltage shifts the output frequency of VCO from f_o to f. On application of error voltage, difference between f_s & f tends to decrease and VCO is said to be locked. While in locked condition, the PLL tracks the changes of frequency of input signal.

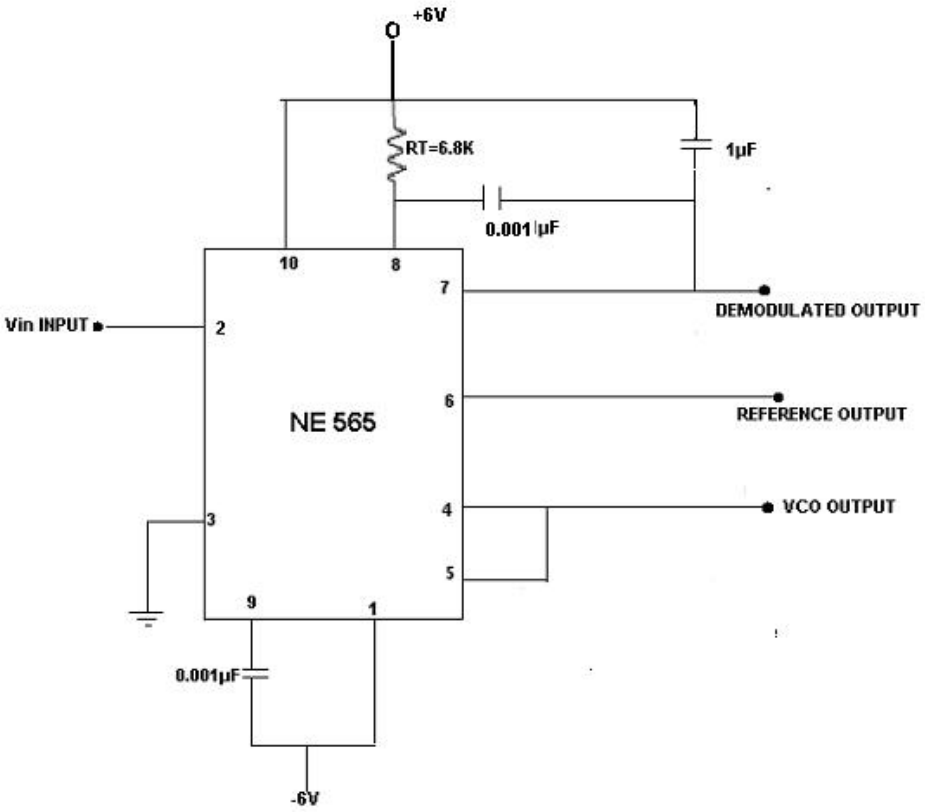
Block Diagram of IC 565



PROCEDURE:

1. Determine the component values using the design procedure given here.
2. Connect the components as shown in the circuit diagram.
3. Note down the readings of output waveform with respect to input signal.

CIRCUIT DIAGRAM:



NE 565 PLL connection diagram

DESIGN PROCEDURE:-

If C= 0.01μF and the frequency of input trigger signal is 2KHz, output pulse width of 555 in Monostable mode is given by

$1.1R_AC = 1.2T = 1.2/f$ $R_A =$

$1.2/(1.1Cf) = 54.5K\Omega$

$f_{IN} = f_{OUT}/N$

Under locked conditions,

$f_{OUT} = Nf_{IN} = 2f_{IN} = 4KHz$

Ex No:12
Date:

PLL CHARACTERISTICS

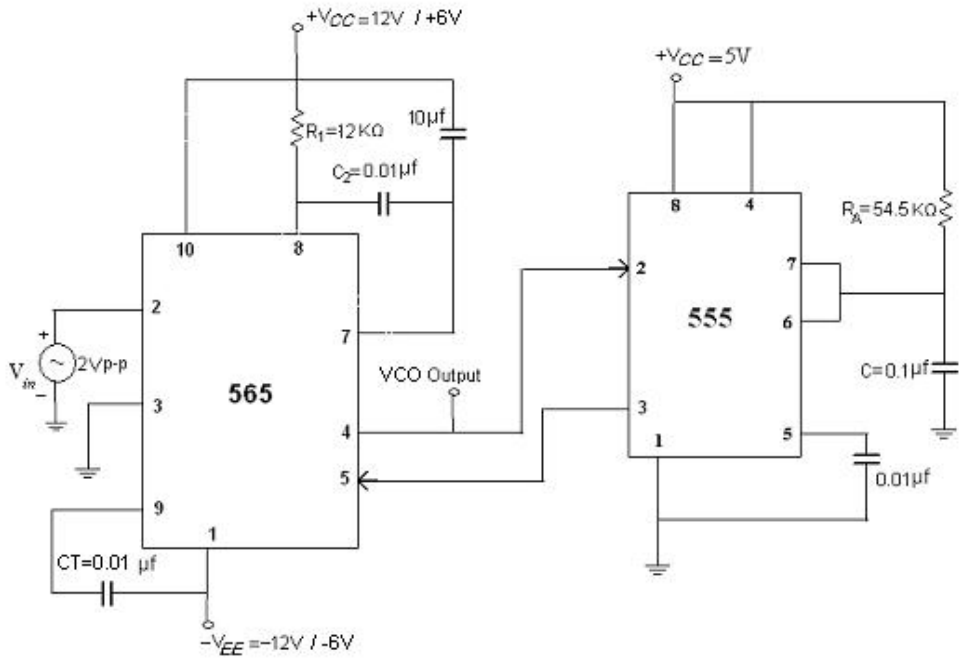
Aim:

To design & test the characteristics of PLL and to construct and test frequency multiplier using PLL IC565.

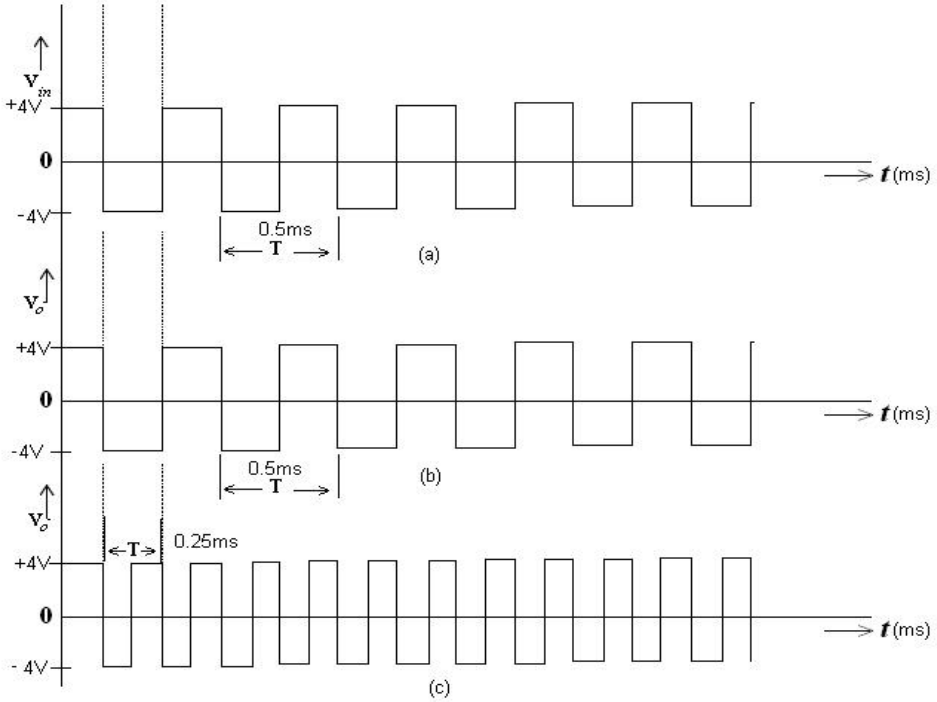
APPARATUS REQUIRED:

S.NO	COMPONENT	VALUE	QUANTITY
1	IC 565	- - -	01
2	IC 555	- - -	01
3	RESISTORS	12KΩ, 54.5 KΩ, 6.8K	Each one
4	CAPACITORS	0.01μF	4
		0.1 μf, 10μf, 1 μf	EACH 01
5	DIGITAL TRAINER KIT	- - -	01
6	REGULATED POWER SUPPLY	(0 -30V), 1A	1
7	CATHODE RAY OSCILLOSCOPE	(0 – 30MHz)	1
8	CONNECTING WIRES	- - -	FEW

.



PLL as Frequency Multiplier



(a): Input

(b): PLL output under locked conditions without 555

(c): Output at pin4 of 565 with 555 connected in the feedback

Theory:

The frequency divider is inserted between the VCO and the phase comparator of PLL. Since the output of the divider is locked to the input frequency f_{IN}, the VCO is actually running at a multiple of the input frequency .The desired amount of multiplication can be obtained by selecting a proper divide– by – N network ,where N is an integer. To obtain the output frequency $f_{OUT}=2f_{IN}$, N = 2 is chosen. One must determine the input frequency range and then adjust the free running frequency f_{OUT} of the VCO by means of R_1 and C_1 so that the output frequency of the divider is midway within the predetermined input frequency range. The output of the VCO now should be $2f_{IN}$. The output of the VCO should be adjusted by varying potentiometer R_1. A small capacitor is connected between pin7 and pin8 to eliminate possible oscillations. Also, capacitor C_2 should be large enough to stabilize the VCO frequency.

SAMPLE READINGS:

PARAMETER	INPUT	OUTPUT
Amplitude (V_{p-p})		
Frequency (KHz)		

PROCEDURE:-

1. The circuit is connected as per the circuit diagram.
2. Apply a square wave input to the pin2 of the 565
3. Observe the output at pin4 of 565 under locked condition.
4. Give the output of 565 to the pin2 of 555 IC.
5. Observe the output of 555 at pin3.
6. Now give the output of 555 as feedback to the pin5 of the 565.
7. Observe the frequency of output signal fo at pin4 of 565 IC.
8. Plot the waveforms in graph.

RESULT:

Thus the PLL characteristics are designed and tested and Frequency multiplier using IC 565 is constructed and tested.

Ex No:13
Date:

STUDY OF SMPS

AIM:

To study the control of SMPS

THEORY:

The switching regulator is also called as switched mode regulator. In this case, the pass transistor is used as a controlled switch and is operated at either cutoff or saturated state. Hence the power transmitted across the pass device is in discrete pulses rather than as a steady current flow. Greater efficiency is achieved since the pass device is operated as a low impedance switch. When the pass device is at cutoff, there is no current and dissipated power. Again when the pass device is in saturation, a negligible voltage drop appears across it and thus dissipates only a small amount of average power, providing maximum current to the load. The efficiency is switched mode power supply is in the range of 70-90%.

A switching power supply is shown in figure. The bridge rectifier and capacitor filters are connected directly to the ac line to give unregulated dc input. The reference regulator is a series pass regulator. Its output serves as a power supply voltage for all other circuits. The transistors Q1, Q2 are alternatively switched „on‟ &; off, these transistors are either fully „on‟ or „cut-off, so they dissipate very little power. These transistors drive the primary of the main transformer. The secondary is centre tapped and full wave rectification is achieved by diodes D1 and D2. This unidirectional square wave is next filtered through a two stage LC filter to produce output voltage Vo.

SG 3524:

FUNCTION:

Switched Mode Power Supply Control Circuit

FEATURES:

- Complete PWM Power Controlled circuitry.
- Single ended or push-pull outputs.
- Line and Load regulation of 0.2%.
- 1% maximum temperature variation.
- Total Supply current is less than 10mA
- Operation beyond 100KHz

RESULT:

Thus the control of SMPS IC SG3524 had been studied.